

**IN THE SPECIFICATION:**

Please amend the specification as follows:

Please replace the paragraph beginning on page 34, line 20 and ending on page 35, line 7, with the following amended paragraph:

This embodiment will be described with reference to FIG. 10. In this figure, only the steps particularly relating to this embodiment are described. The steps from FIGS. 10A to 10C describe formation of isolation trench 2, formation of p-type well 3 and n-type well 4, formation of gate electrode, formation of silicon films of n-type ~~region~~ silicon film 14n and p-type ~~region~~ silicon film 14p, formation of  $WN_x$  film 24 and W film 25 (FIG. 10A), formation of silicon nitride film 29 (FIG. 10B), and patterning the silicon nitride 29 by photolithography (FIG. 10C). In the first embodiment, the silicon nitride film 29 located at the boundary connecting n-type impurity and p-type impurity regions of the amorphous silicon film, is processed to make patterns, and then, using the patterned silicon nitride 29 as a dry-etching mask,  $WN_x$  film 24 and W film 25 of this region are removed.

Please replace the paragraph beginning on page 35, line 8 and ending on page 36, line 3, with the following amended paragraph:

In this embodiment, carbon 73 is doped in the W film 25 and  $WN_x$  film 24 by an ion implantation technique using the silicon nitride film 29 as a mask except for removing the W film 25 and  $WN_x$  film 24. The carbon implantation was carried out with dosage of  $1 \times 10^{16} / \text{cm}^2$  at 5 keV. By heat-treatment in nitrogen atmosphere at 650.degree. C. for 10 minutes, the area of ion implanted W film 25 and  $WN_x$  film 24 changed into metal carbide 74 (FIG. 11A). After that, silicon nitride film 34 was deposited to be 120 nm in thickness by a plasma CVD method and, using this film, W film 25 and  $WN_x$  film 24 and n-type silicon film 14n and p-type silicon film 14p were processed to make the gate electrode and wiring pattern. The side wall spacer 11s was formed along the wall of the gate electrode similar to the gate (FIG. 11B) described in the first embodiment, and a silicon oxide film is deposited to make the insulating interlayer 40. Subsequently, the contact plug 23 consisting of a complex of Ti/TiN/W is formed, and then wiring 33 comprising a laminate structure of a. W film 69 deposited by a sputter method and a W film deposited by a CVD method was formed on the insulating interlayer 40 (FIG. 11C). Titanium nitride 35 may be

used to connect W film 25 and  $WN_x$  film 24 isolated by the metal carbide 74 (FIG. 1D). The top plan view is shown in FIG. 22B.